IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Stephen H Tang et al.

Title: FLOATING-BODY DRAM WITH TWO-PHASE WRITE

Docket No.:	80107.038US1	Serial No.:	10/716755
Filed:	November 19, 2003	Due Date:	N/A
Examiner:	Unknown	Group Art Unit:	2818

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.
X An Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.), and copies of 6 cited documents.

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 50-2359.

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By: Dana B. LeMoine
Atty: Dana LeMoine
Reg. No. 40,062

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 5 day of March, 2004.

Emily Bates
Name

Emily Bates
Signature

(GENERAL)

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Serial No.:	10/716755	Group Art Unit:	2818
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Title:	FLOATING-BODY DRAM WITH TWO-PHASE WRITE		
Assignee:	Intel Corporation		

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 50-2359 in order to have this Information Disclosure Statement considered.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

STEPHEN H TANG ET AL.

By their Representatives,

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Date 3-5-04 By Dana B. LeMoine
Dana LeMoine
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known

Application Number	10/716755
Filing Date	November 19, 2003
First Named Inventor	Tang, Stephen
Group Art Unit	2818
Examiner Name	Unknown
Attorney Docket No:	80107.038US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		FAZAN, PIERRE, et al., "A Simple 1-Transistor Capacitor-Less Memory Cell for High Performance Embedded DRAMs", IEEE 2002 Custom Integrated Circuits Conference, (2002),99-102	
		OHSAWA, TAKASHI, et al., "A Memory Using One-Transistor Gain Cell on SOI(FBC) with Performance Suitable for Embedded DRAM's", 2003 Symposium on VLSI Circuits Digest of Technical Papers, (2003),4 pages	
		OHSAWA, TAKASHI, et al., "Memory Design Using a One-Transistor Gain Cell on SOI", IEEE Journal of Solid-State Circuits, vol. 37, no. 11, (November 2002),1510-1522	
		OHSAWA, TAKASHI, et al., "Memory Design Using One-Transistor Gain Cell on SOI", ISSCC 2002, Session 9, Dram and Ferroelectric Memories, 9.1, (February 5, 2002),3 pages	
		OKHONIN, S., "A Capacitor-Less 1T-DRAM Cell", IEEE Electron Device Letters, vol. 23, no. 2, (February 2002),85-87	
		OKHONIN, S., et al., "A SOI Capacitor-less 1T-DRAM Concept", 2001 IEEE International SOI Conference, (October 2001),153-154	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached